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10/608,747	06/27/2003	Dinh Bui	53597.1501	7706

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2005 MARKET STREET, SUITE 2200
PHILADELPHIA, PA 19103-7013

EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/608,747	BUI ET AL.
	Examiner	Art Unit
	Linh M. Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9,10,12,13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5* is/are allowed.

6)☒ Claim(s) *2-4,6,7,9,10,12,13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to Applicants' amendment filed 07/06/2004. By virtue of this amendment, claims 1, 8, 11, 14 and 21 are canceled; thus claims 2-7, 9-10, 12-13 and 15-20 are currently pending in this application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2-4 and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Klein et al. (U.S. Patent No. 4,694,257).

With respect to claim 2, Klein et al. discloses, in Figure 2, a semiconductor device comprising a) an integrated circuit buffer [12, 20, 22, 14, 16, 18] having a delay generator [12, 22, 14, 16], the buffer receiving an input signal [RX] and generating a plurality of output signals [outputs from 18] that relate to the input signal, the delay generator being configured to phase-shift the timing of the plurality of output signals with respect to the input signal; and a resistor [20] having a resistance value, a first resistor end that is electrically connected to the delay generator and a second resistor end that is electrically connected to ground or a voltage reference [Vcc], wherein the resistor is external to the integrated circuit buffer, the resistance value determining a magnitude of the phase-shift caused by the delay generator *(inherently, current, I, from Vcc/Rt goes directly to item 14 and therefore affect the phase shift resulted in the output of*

PLL 18, obviously current I varies as the resistance value of Rt varies which in turn influences the phase shift of output of PLL 18).

With respect to claim 3, Klein et al. discloses, in Figure 2, that the buffer comprises a zero-delay buffer.

With respect to claim 4, Klein et al. discloses, in Figure 2, the device is implemented on a circuit board and the external resistor is connected to a pin on a device package.

With respect to claim 15, Klein et al. discloses, in Figure 2, a circuit and its corresponding method of adjusting the timing of an output signal of a semiconductor device comprising the steps of a) electrically connecting a first terminal of an external resistor [20] to a buffer that generates a plurality of output signals [outputs from 18], the external resistor having a resistance value and the buffer including a delay generator [12, 22, 14, 16] and a phase locked loop [18], the first terminal of the external resistor being electrically coupled to the delay generator; and b) electrically connecting a second terminal of the external resistor to a ground or a voltage reference [Vcc], c) receiving a clock input signal [RX signal] in the buffer; and d) phase shifting the timing of one or more of the output signals [output form 18] in an amount that is dependent upon the value of the external resistor *(inherently, current, I, from Vcc/Rt goes directly to item 14 and therefore affect the phase shift resulted in the output of PLL 18, obviously current I varies as the resistance value of Rt varies which in turn influences the phase shift of output of PLL 18).*

With respect to claim 16, Klein et al. discloses, in Figure 2, that the buffer comprises a zero-delay buffer.

With respect to claim 17, Klein et al. discloses, in Figure 2, a semiconductor device, comprising a) an input terminal that receives an input signal [RX], b) a buffer [12, 20, 22, 14, 16, 18] that receives the input signal from the input terminal which is configured to generate a plurality of output signals and to phase-shift the timing of at least one of the plurality of output signals with respect to the input signal; and c) an external resistor [20] coupled between the buffer and ground or a voltage reference [Vcc], the external resistor having a resistance value that determine a magnitude of the phase-shift of at least one of the plurality of output signals relative to the input signal *(inherently, current, I, from Vcc/Rt goes directly to item 14 and therefore affect the phase shift resulted in the output of PLL 18, obviously current I varies as the resistance value of Rt varies which in turn influences the phase shift of output of PLL 18).*

With respect to claim 18, Klein et al. discloses, in Figure 2, that the buffer comprises a zero-delay buffer.

With respect to claim 19, Klein et al. discloses, in Figure 2, that the device is implemented on a circuit board and the external resistor is connected to a pin on a package of the device.

With respect to claim 20, Klein et al. discloses, in Figure 2, that the at least one of the plurality of output signals are phase-shifted to have a timing that is advanced or retarded relative to the input signal and the remaining output signals.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-7, 9-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein et al. (U.S. Patent No. 4,694,257) in view of Andresen et al. (U.S. Patent No. 5,355,037).

With respect to claims 6, 9, and 12, Klein et al. discloses all of the claimed limitations as expressly recited in claim 1, except for a) the phase locked loop includes a phase detector; and b) the delay generator, a delay line and the external resistor are electrically connected to adjust the timing of an internal feedback signal before the feedback signal reaches the phase detector.

Andresen et al. discloses, in Fig. 1, a phase locked loop with details including a) a phase detector, b) delay line and c) an internal feedback signal.

To configure the circuit of Klein et al. with a phase locked loop including details as taught by Andresen et al. having a phase detector, a delay line and an internal feedback to achieve high performance would have been obvious to one of ordinary skill in the art at the time of the invention since Andresen teaches that such configuration would facilitate high frequency clock synchronization *(see Andresen et al., col. 1, lines 6-9).*

With respect to claims 7, 10 and 13, the combined teachings of Klein et al. (Fig. 2) and Andresen et al. (Fig. 2), disclose that the plurality of output signals are phase-shifted to have a timing that is advanced relative to the input signal.

Allowable Subject Matter

5. Claim 5 is allowed.

6. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest: A semiconductor device including a plurality of internal capacitors which are used in conjunction with an external resistor for providing a timing reference, each capacitor having a first capacitor end that is electrically connected to a current source and a second capacitor end that is electrically connected to ground or a voltage reference, as called for in claim 5.

Remarks and Conclusion

7. Applicants' argument filed 07/06/2004 have been fully considered by they are not persuasive.

With respect to the Applicants' argument on claim 2, at page 9, first paragraph, the examiner disagrees with the Applicants' statement of *"Klein fails to disclose or suggest a semiconductor that includes an integrated circuit buffer having a delay generator that is configured to phase-shift the timing of a plurality of output signals with respect to an input signal and a resistor which is external to the buffer and which has a resistance value that determines a magnitude of the phase-shift caused by the delay generator."*. Klein inherently discloses, in Fig. 2, that current, I, from Vcc/Rt goes directly to item 14 and therefore affect the phase shift resulted in the output of PLL 18; obviously, current I varies as the resistance value of Rt varies which in turn influences the phase shift of output of PLL 18.

With respect to the Applicants' similar argument on claim 15, at page 10, first paragraph, see response to claim 1's argument in the above paragraph.

With respect to the Applicants' similar argument on claim 17, at page 11, see response to claim 1's argument in the above paragraph.

With respect to the Applicants' similar argument on claims 6-7, 9-10 and 12-13 regarding dependency on claim 2, at page 12, last paragraph bridging page 13, see response to claim 1's argument in the above paragraph.

Still with respect to the Applicants' argument on claims 6-7, 9-10 and 12-13, at page 13, first full paragraph, the examiner disagrees with the statement *"modification or combination of the prior art would change the principle of operation of prior art invention"*. The combination of Klein et al. and Andresen et al. is very obvious to one of ordinary kills in the art since Klein et al. lacks showing the details of the phase locked loop and Andresen et al. discloses the details including all the typical element of a phase locked loop a phase detector, a delay line and an internal feedback. Thus combination of Klein et al. and Andresen et al. would not change the principle of operation.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER